Design of a Digital Clock Using Very High Speed IC Hardware Description Language

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Abstract -- **Very High Speed IC Hardware Description Language (VHDL) is one of the modern languages used in designing digital circuits. It can be used in programming Field Programmable gate arrays (FPGAs) and Application Specific Integrated Circuits (ASICs).This paper presents the design of a digital clock using Very High Speed Hardware Description Language in a Xilinx ISE 10.1 environment. The designed clock has the functionalities time, alarm, stopwatch and date. The clock format can be changed from 24 hours to 12 hours and vice versa. After the design, testing was done on a Spartan-3- FPGA and all units were found to be performing the desired functions.**

Keywords: VHDL, Programmable Logic Devices, FPGA

I. INTRODUCTION

THERE are different digital logic integrated circuits available in the market. These can be used in designing circuits by circuit designers. But as systems become complex, there may be some functions that cannot be performed by these readily available ICs. Hence the use of VHDL for circuit design comes in handy [1]. VHDL is a high level programming language which is powerful in programming Programmable Logic devices such as field programmable gate arrays, generic array logic (GAL) and Programmable array logic [2],[3]. For the programmable logic devices to be programmed the codes must pass through stages such as synthesis, timing simulations, place and route and bit file generation [4]. This work will be based on design on an FPGA. The advantage of designing digital circuits used for instrumentation and control using it is that the circuits can be modified even after reaching the market due to the reprogrammability of FPGAs thereby enhancing rapid prototyping [5]. There are many manufacturers of FPGA such as Xilinx; Inc, Altera Corporation, Perfect Parts Corporation, Achronix Semiconductor Corporation, Atmel Corporation [6], [7] etc. FPGAs' contain programmable logic elements called Logic elements LEs' and a hierarchy of reconfigurable interconnects that allow Les' to be connected physically [5]. In this work, a Spartan-3 FPGA development board is used. The designed circuit has the following features:

The Clock: This is designed to display time in the format hr: min: sec. System clock is scaled down to 1Hz to trigger the clock and other components. The seconds count after each clock pulse till it reaches 59 and on the next system clock pulse it resets back to 0 and then continues. At the time it resets to 0, it triggers the minute. Each time the seconds reset to 0, the minute is being triggered and when it reaches 59, it triggers the hour, the next time it is triggered by the seconds.

Five switches "stop", "settime", "sethr", "setmin" and "inct" are used for resetting time. To achieve this, the clock has to be stopped by first setting the "stop" switch to logic '1' followed by the "settime" switch. Then either "sethr" or "setmin" can be set high to reset the hour and minute respectively. If sethr is set high, it means that the hour will be changed. The next thing to do is to press the "inct" button (increment button). User can continue incrementing it up to the value of 23 after which it resets to 0 and the incrementing process can be continued.

The same principle is used to reset minutes using "setmin". But in this case it reaches a maximum of 59 before resetting. Time format can be changed by setting the "format" switch to either logic '1' or '0'. When set to logic '1', the digital clock will be in 24 hours mode while when set to '0', it will be in 12 hours mode, which can reach a maximum of 11 hours.

Option switches are used for selecting the variable either time, date, alarm and stopwatch to be displayed by the seven segments display unit of the Spartan-3 FPGA. The options are four in number with each enabling one of the mentioned variables. Only one of them has to be high at a time so as to enable the variable assigned to be displayed.

The minutes are displayed by two seven segment display LEDs' of the Spartan-3 FPGA [8] and hour by the other two. Seconds are displayed by six LEDs' which presents it in a binary form with off state represented by a '0' and on state by a '1'.

The Stopwatch: This is activated by setting a "strtstop" slide switch to logic level '1' and stopped by setting it to logic '0'. The stop watch can be run for 60 minutes only. When it reaches 59 it resets to 0 seconds and zero minutes on the next clock cycle. Before activating the stopwatch, the correct option

button has to be activated for it to be displayed on the seven segments display unit. The first two seven segment LEDS gives the seconds count and others give the minutes count.

The Alarm: The alarm has a switch "setalm". When the button is set, user can set and adjust the alarm setting using "sethr", "setmin" and "inct". At the time when the alarm set time becomes equal to the clock time, an output pulse is sent out. This is dependant on whether a 24 hours or 12 hours format is selected. User adjusts it by taking into consideration which time format is used at a particular moment.

The Date: This has a value of 0 to 31 which increments at the end of each 24 hours. It can be adjusted using an "Adate" switch provided. When the "Adate" switch is set high, user can use the "Inct" button to increment it. Before adjusting, the "stop" button has to be set high and the option button representing date display most also be high. The maximum it can reach is 31 which then resets to 0.

II. METHODOLOGY

The codes for the functionalities mentioned earlier were written in eight different files and were assigned names listed below:
1. Tb_toplevel.vhd
2. Toplevel.vhd
3. Clockdivider.vhd
4. Clock.vhd
5. Alarm.vhd
6. Stop.vhd
7. Date.vhd
8. Scan4digit.vhd

- Tb_tplevel.vhd is a test bench file for the entire digital clock design.
- Toplevel.vhd is the top level of the design and it includes six components.
- Clock Divider.vhd is a file that provides the clock pulse needed by all components in this work. The Spartan-3 FPGA is set to operate at a frequency of 50MHz. This frequency cannot be used for setting the timings in the digital clock, and so there is the need to reduce it to 1Hz. To do this, the board oscillator frequency is divided by 50×10^6 to obtain a frequency of 1Hz. This is done by setting a variable "count" and then increments its value up to 50000000, covering 50×10^6 cycles. At the end of the 50 million cycles, it sends a pulse to the remaining component parts. The variable count resets to 0 and the process continues.
- Clock.vhd contains the codes describing the functionalities of the clock.
- Alarm.vhd describes the components of the alarm.
- Date.vhd describes the function of the date.
- Stop.vhd is for the stopwatch.
- Scan4digit.vhd acts as a decoder that receives an input

signal from the various components and determine the
- Spartan-3 seven segment display on which to display each digit.

The top level consists of 7 segment display decoders for displaying the signals from all components in the system on a seven segment display. It receives a six bit input data and converts it to a form that represents the binary number on a common anode seven segment display. The seven segment display of each of the variables time, alarm, stop watch and date were generated separately.

Codes for interchanging between one display mode and the other were included in the top level.
A new project was created using Xilinx ISE 8.2i with name "mydigitalclock". The eight source files mentioned earlier were added. Relationship between the files was established through portmaps and signals in the top level. Each file was saved and synthesis was carried out. Some minor errors were debugged and the synthesis stage was passed. The register transfer logic was generated, pins were assigned using [8] as reference and finally the bit file was generated. The bit file was programmed onto the Spartan-3 FPGA and testing was performed which proved that the design is well done.
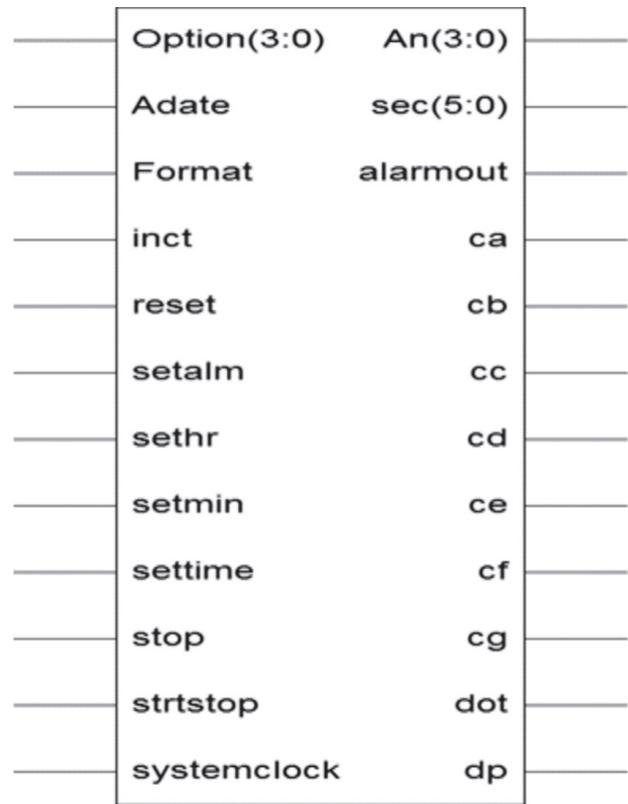
III. RESULTS

Figure 1. Register Transfer Level of the digital clock.

The table below shows how the resources in the Spartan-3 FPGA were utilized:

TABLE 1: SPARTAN-3 FPGA RESOURCES UTILIZATION

Logic Utilization	Used	Available	Utilization
Total Number Slice Registers	124	3,840	3%
Number Used as Flip flops	98		
Number Used as Latches	26		
Number of 4 Input LUTS	444	3,840	11%
Logic Distribution			
Number of Occupied Slices	259	1,920	13%
Number of Slices Containing Only Related Logic	259	259	100%
Number of Slices Containing Unrelated Logic	0	259	0%
Total Number of 4 Input LUTS	485	3,840	12%
Number Used as Logic	444		
Number Used as route-thru	41		
Number of Bonded IOBs	35	173	20%
Number of BUFGMUXs	3	8	37%

IV. CONCLUSION

The Digital Clock was designed by first creating VHDL codes and synthesizing them using Xilinx ISE 8.2i software. The codes passed synthesis and a bit file was generated. The bit file was programmed onto a Spartan-3 development kit and tested for functionality. The circuit performed the desired functions. Design statistics also showed that the FPGA resources were highly utilized and therefore the design is economical. This proves how FPGAs are desirable when dealing with complex systems.

V. REFERENCES

[1]. M. Balch, *Complete Digital Design; A Comprehensive Guide to Digital Electronics and Computer Systems Architecture*, Mc Graw Hill, 2003, pp 221-222.

[2]. B. Holdsworth and C. Woods, *Digital Logic Design* (fourth edition), Newnes, 2002, pp 295-324.

[3]. J.F. Wakerly, *Digital Design Principles and Practices*, Prentice Hall, 2005, pp 15-16.

[4]. Enoch O.H., *Digital Logic and Microprocessor Design with VHDL*, Lasiera University, 2006, pp 23-26.

[5]. http://www.altera.com/products/fpga, accessed 15th July, 2014.

[6]. http://www.globalspec.com/local/3127/CA, accessed 15th July, 2014.

[7]. http://www.xilinx.com/index.htm, accessed 15th July, 2014.

[8]. Nexys Reference Manual.

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