Circuit Architecture for Photon Counting Pixel Detector with Threshold Correction

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Abstract -- **In the hybrid pixel detectors, the detector and the readout circuit are constructed separately and then connected electrically by flip-chip bonding. This concept allows the same readout chip to operate using different sensor materials. In photon counting readout, it takes into account the noise around the signal, and other effects such as the variation of amplifier gain and the signal offset. To have a good efficiency for the signals charge, the comparator threshold setting is needed to be low enough. In this paper, a photon counting pixel detector readout with threshold correction is implemented as a solution for the missing counting of the signal due to the offset problem. The additional circuits needed for this architecture, lead to an increase in power consumption and only a marginal increase in circuit area. It is implemented in a 120-nm CMOS process and the presented results are based on simulations.**

Keywords: *Threshold, Photon-Counting, Pixel, Noise, Discriminator.*

I. INTRODUCTION

READOUT circuits for photon counting image sensors are based on analog and digital circuits, such as the Medipix 2 [1]. Photon-counting pixels contain complex circuitry, which means that the pixel design is mainly driven by area, power consumption and mixed mode design constraints. In photon counting pixel readout of X-rays if a pixel does not have excellent X-ray sensitivity, a low energy threshold and a low noise contribution, then attempts to correct intensity measurements may fail because small changes in threshold can lead to significant alteration in detection efficiency. Because small variations in threshold make it very difficult to avoid missing counts. To solve this problem four discriminators per pixel instead of double discriminators are used. For low discriminator level, the circuit consists of sum circuit and two comparators, one of the comparator work as a threshold correction. For high discriminator level, the circuit consists of two comparators and (AND gate). For improving threshold uniformity, the circuit is equipped with two 5-bits analog to digital converters DACs. One of the DAC is used to bias the feedback transistors of the preamplifier and the shaper. The second DAC set the threshold voltages Th_{LL}, Th_{LH}, Th_{HL}, and Th_{HH} in the comparators see (Figure 1).

II. METHODOLOGY

A block diagram of the circuit architecture of Photon counting readout with the threshold correction is shown in Figure 1. The circuit contains an analog signal processing and digital circuitry. The analog parts consists of a charge sensitive amplifier; a shaping filter, four discriminators and include pile-up rejecters, as the design of this circuit involved a 120nm CMOS process using a power supply voltage of 1.2 V. In this case a current mode circuit was used which means that the signals are represented by a current. The current mode circuits could be a better choice as the power supply voltages are lowered, since the signal swing is indirectly limited by a reduction of the available supply voltage range [2]. The digital part consists of (AND gate), Sum circuit, All Digital Window Discriminator (ADWD) and an event counter.

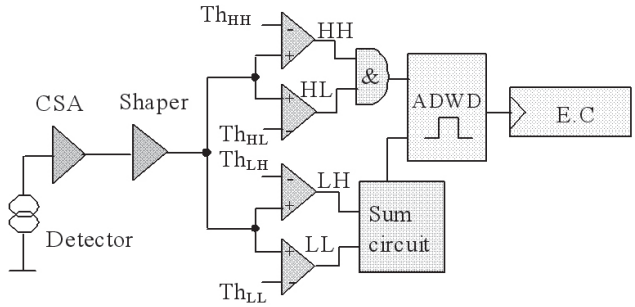

Figure 1. Simplified block diagram of the photon counting pixel readout.

Charge Sensitive Pre-Amplifier: The charge sensitive amplifier (CSA) is widely used at the front-end electronics in radiation detectors as its conversion gain is independent of anode capacitance variation because the charge released by the detector is directly integrated on the feedback capacitor [3]. Then its gain is not sensitive to a charge in detector capacitance. The CSA is a cascade structure as shown in Figure 2 has a peaking time of 20ns and a bandwidth of 2.8 MHz at 3-dB and a gain of 25. In terms of power consumption the CSA uses 840 nW in the active mode. The input transistor M1 is nMOS transistor with minimum channel length, in order to minimize series white noise the width of transistor is selected to give minimum noise [4]. The bias input current is fed at the gate of transistor M1 falls within the range of 100 nA. Transistor M2 constitutes the cascade. Current is supplied to the M1 node

via a cascade current source (M4 and M3), which sets M1 in the region of operation [5]. Transistors M2, M3 and M4 are externally biased. In order to drive a low-impedance load, double source followers, transistors (M5 - M8) are used in this design to provide a low-impedance output to drive the following pulse shaper stage. The main noise contribution to the total noise of the preamplifier comes from the M1 input, although the noise contribution from the cascade current source is not negligible due to the low power supply and the limited voltage available to degenerate them [6]. The discharging feedback resistor is formed by the drain-source resistance (Rds) of transistor Mf, which is biased by the current DAC to operate in the saturation in quiescent conditions and it enters in strong inversion when a charge signal is detected [7].

The frequency behavior of the CSA is determined by the feedback capacitor Cf and the total parasitic capacitance on the high input impedance node. This capacitance consists of the parallel combination of drain capacitances of transistors M3 and M4, input capacitance and gate capacitance of the subsequent stages.

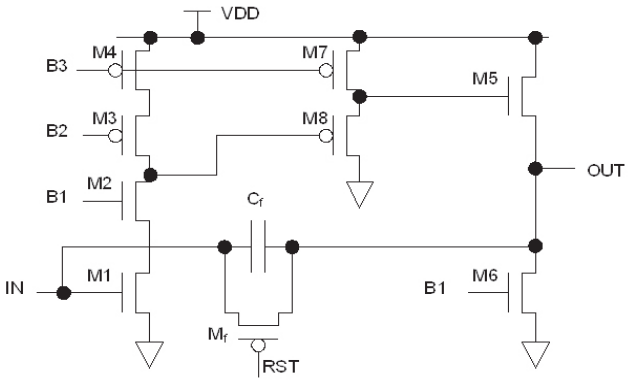

Figure 2. Circuit diagram for pre-amplifier.

Pulse Shaper: The signal detected by the CSA in photon counting readout electronics will generally not be used directly, but will be amplified and shaped. The aim of these procedures is to optimize the signal to noise ratio [8].

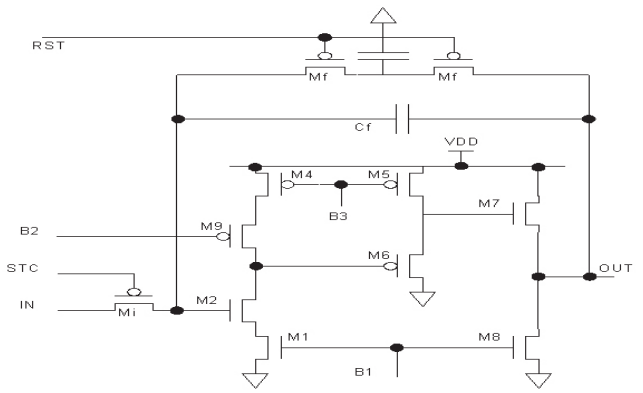

Figure 3. Circuit diagram of pulse shaper.

The selected pulse shaper must remove low and high frequencies to control signal pile-up and limit the band width. However, while improving the output noise level by limiting the bandwidth, pulse shaping without gain will result in loss of signal and may possibly not provide any real improvement to the output SNR. The amplifier used in the pulse shaper is the same as the one used in the CSA. It is a cascade structure as shown in Fig. 3.

The pulse shaper amplifier has a shaping time of less than 250ns and a bandwidth of 2.4MHz. The simulated noise figure is 42 dB less than CSA as expected; the noise figure is greatly reduced by the pulse shaper. The input transistor M2 receives the signal from CSA via transistor Mi. Current is supplied to the M2 node via a cascade current source (M4 and M9). The second stage of the pulse shaper (not discussed in this paper) consists of a push-pull cascade current source amplifier. In figure 3, the output signal OUT of the pulse shaper is fed to a push-pull cascade current source amplifier. In term of power consumption the first stage of pulse shaper uses 246nW in the active mode whereas the second stage increases the power consumption. The shaping time is controlled by the drain-source resistance Rds of the PMOS transistor Mi which is biased by the signal STC that comes from external current mirror. Bias voltages (B1, B2, and B3) come from a bias network, which is common to preamplifier, shaper and comparators. Mf is controlled by the current DAC that allows adjustment of the current simultaneously by the external current.

Comparator: In photon counting X-ray imaging the signals appear randomly in time and independently in each pixel. After receiving a charge signal from the detector, and having been integrated and shaped, there is a requirement to implement a threshold discriminator in each pixel. In X-ray imaging techniques it is sufficient to measure the spatial distributions of the X-rays of energies above a given threshold (integral discriminator type) or within a given energy window (window discriminator).

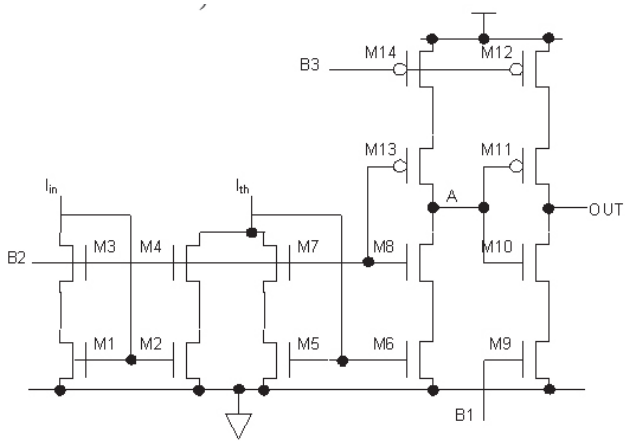

Figure 4. Schematic diagram of comparator.

In the integral discriminator, a comparator outputs a logical signal every time the amplitude exceeds a preset threshold. This is the main feature characterizing the single photon counting in comparison to an integrating pixel. This is because the signal amplitude at the shaper output contains information about the charge generated in the detector [3]. In the window discriminator type, two comparators are used to output appropriate pulses when the input exceeds a lower threshold and is below an upper threshold.

The comparator is implemented as a cascade current differential amplifier, see Fig. 4. The circuit, made up of the transistors M1 – M8, consists of low voltage cascade current mirrors with the output current of the first subtracting from the input of the second. The current in point A equal (Iin - Ith). Where Iin is the input current from pulse shaper and Ith is the threshold current setting by the current DAC. The value of the subtracting current is fed to the push-pull cascade current source, transistors (M9 -M14) to generate a voltage output pulse.

Sum circuit: The schematic of the Sum current circuit is based on the current-mode CMOS multiple valued logic circuits [10], is shown in Figure 5. The circuit received two clock signals from comparators it form lower threshold discriminators LL and LH that drive PMOS switch transistors M6 and M7. The sum of signals is the threshold value. NMOS transistors M4, M5 each provide current to PMOS switches M6 and M7 that are controlled by signal LL and LH respectively. These two low-level currents thresholds are summed at the drain of PMOS transistor M17. This current is fed to the double push-pull cascade current source, transistors (M8 -M15) in order to generate a voltage output pulse.

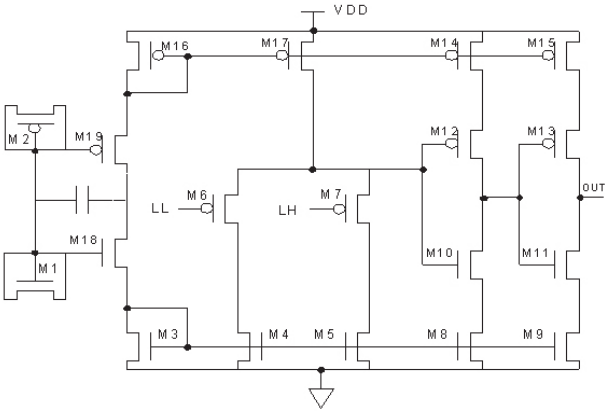

Figure 5. Schematic diagram of sum circuit.

Figure 6 shows a simplified block diagram of the 4 comparators threshold setting. The signals ThLL and ThHL are the threshold setting at the normal state (no offset), and the signals with dotted lines ThLH and ThHH are the threshold setting at the offset state.

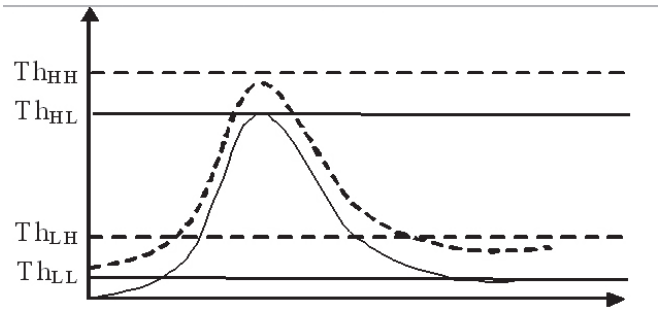

Figure 6. Block diagram of the thresholds setting.

D/A Converter: In the mode of D/A converter, voltage, current and charge, the current mode conversion in conversion rate has the advantage that voltage swings in the circuit are minimized, which ultimately reduces the sensitivity for parasitic capacitance. In our design, we chose current mode conversion for R-2R ladder D/A converter. The basic structure of digital-to-analog converter is R-2R configuration. Since CMOS switch is not ideal, the resistance of switch affects the accuracy of R-2R network, we adopt CMOS transistors to replace R-2R resistors. CMOS R-2R ladder is based on a linear current division principle [11].

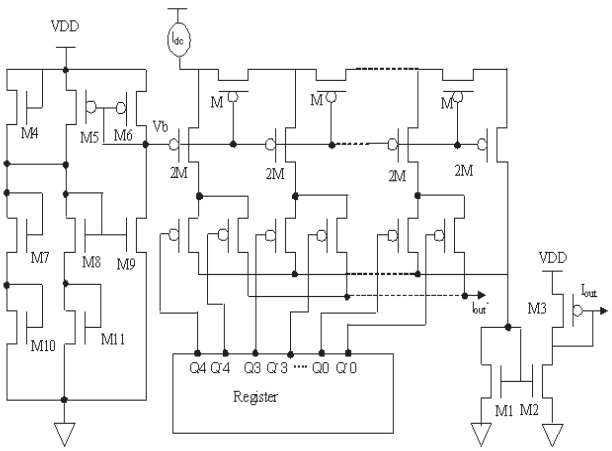

Figure 7. Block schematic of the 5-bit current DAC.

The input current supplies a current source for R-2R network, which is similar to the classical R-2R resistor ladder which normally requires a large area and bigger power consumption. We use CMOS transistors instead of polysilicon resistors to reduce the area and power consumption. The linking Iout and Iout- ports not only act as resistors, but also as switches, so that this structure solves the problem of additional resistance of switch. Figure 7 shows 5-bit DAC schematic of R-2R transistor ladder, which is biased by a reference current source. Vb is the voltage which equals the output voltage of signal data (D0 - D4), and the low voltage of data is below the threshold voltage of CMOS transistors. Iout is the output current of ladder. Iout- is the dump current of ladder.

III. SIMULATION RESULTS

The complete circuit was simulated in a 120 nm CMOS process. Both analog and digital circuitry have been designed to operate with 1.2 V power supply.

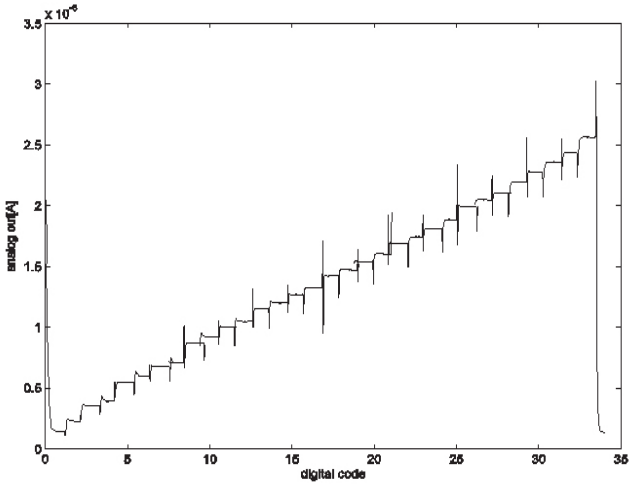

Figure 8. Simulation of 5-bit DAC.

In the DAC we used current mirror as the output stage. The DAC supply their output currents directly to the current mirrors M1, M2, M3 (Figure 7). Due to the channel modulation effects, the effective ratio of the drain current in M1 and M2 depends on drain-source voltages of both transistors, which are functions of the current fed into transistor M1 and the load transistor M3. Figure 8 shows the output current of the DAC with differential nonlinearity and integral nonlinearity error in Figure 9.

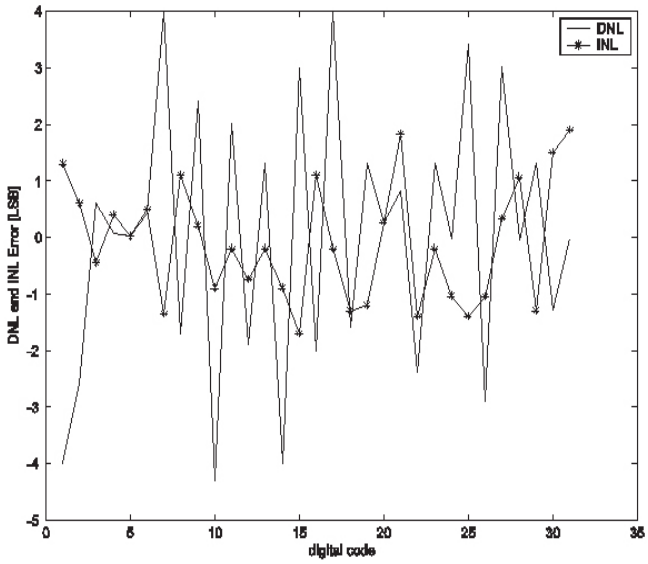

Figure 9. Differential and integral nonlinearity errors.

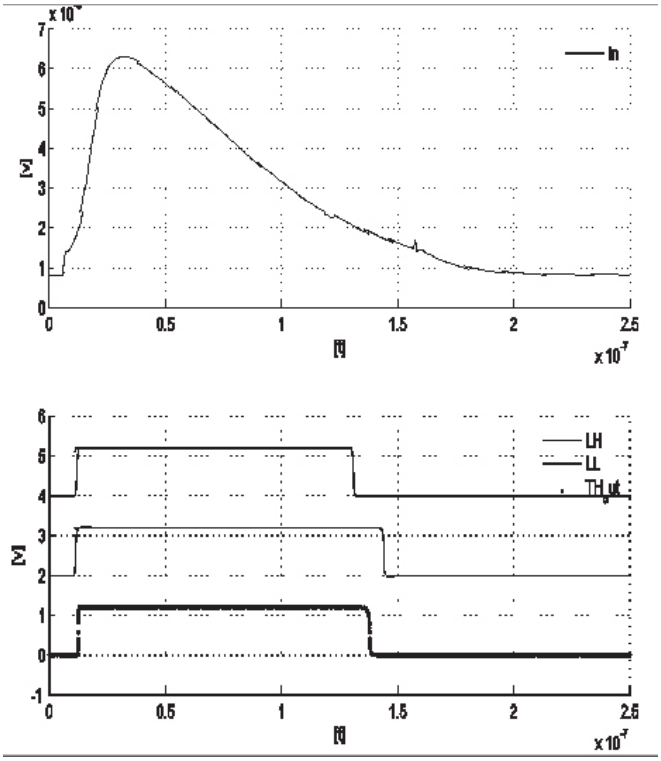

Figure 10. Simulation result of the circuit without offset input signal.

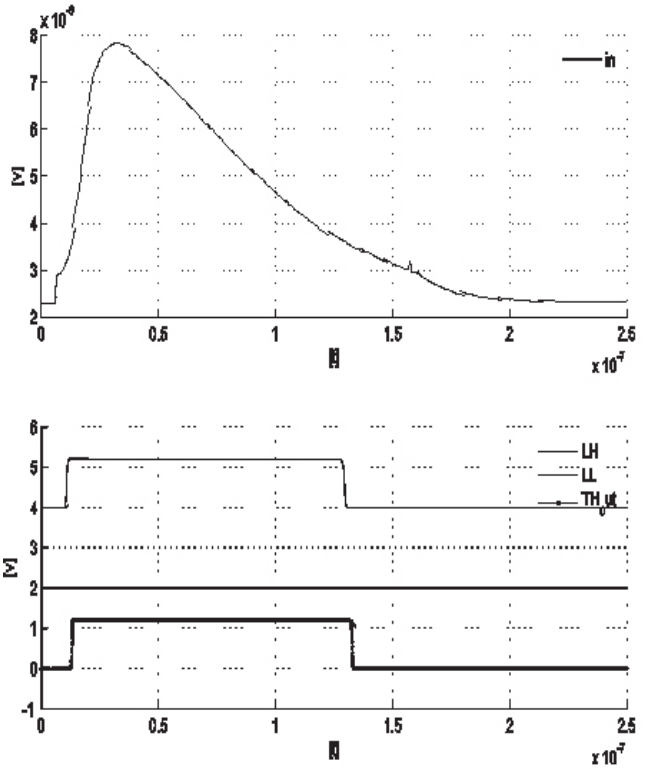

Figure 11. Simulation result of the circuit with offset input signal.

Simulation result of the sum circuit at the lowers discriminator setting, when the shaper signals without offset as shown in Figure 10. The discriminator generates two clock signals LL and LH that are input to the sum circuit, the output from the sum circuit is almost less than LL signal and bigger than LH. Figure 11 shows the clock signal when shaper signal include offset.

IV. CONCLUSION

In this paper we have introduced architecture for a photon counting pixel detector readout with threshold correction for the comparators is implemented as a solution for the missing counting of the signal due to the offset problem. The additional circuits needed for this architecture, leads to an increase in power consumption and in circuit area. It is implemented in a 120nm CMOS process and the presented results are based on simulations.

V. REFERENCES

[1]. X. Llopart, M. Campbell, R. Dinapoli, D. san Segundo and E. Pernigotti, "Medipix2, a 64k pixel readout chip with 55 µm square elements working in single photon counting mode", *IEEE Transactions on Nuclear Science*, Vol. 49, pp. 2279-2283, October 2002.

[2]. Bengt E. Jonsson "*Switched-Current Signal Processing and A/D Conversion Circuits- Design and Implementation"*, ISBN 0-7923-7871-7.

[3]. Suliman Abdalla, Bengt Oelmann, Mattias O'Nils, Jan Lundgren, "Architecture and Circuit Design for Colour X-ray Pixel Array Detector Read-out Electronics", *Proceedings of the IEEE Norchip Conference,* pp. 271-276, 2006.

[4]. P. O'Connor et al., "Readout Electronics for a High-Rate CSC Detector," Fifth Workshop on Electronics for LHC Experiments, Snowmass Colorado, September 1999.

[5]. M. A. Abdalla, C. Fröjdh, C.S. Petersson, "A New Biasing Method for CMOS Preamplifier-Shaper," *Proc. Of the 7th IEEE Intl. Conf. on Electronics Circuits and Systems*, pp. 15-18, 2000.

[6]. P. O'Connor and G. De Geronimo, "Prospects for charge sensitive amplifiers in scaled CMOS," in *IEEE Nuclear Science Symp. Conf. Record*, Vol. 1, Oct. 1999, pp. 89–93

[7]. M. Pedrali, *et al.,* "PETRIC- A Positron Emission Tomography Readout Integrated Circuit," *IEEE Transactions on Nuclear Science*, Vol. 48, No. 3, June 2001

[1] Larry T, Wurtz and W. Perry Wheless, "Pulse Shaping for Low-Noise, Charge Preamplifiers," *IEEE Transaction and Measurement*. Vol. 42, No. 5, October 1993

[2] B. Oelmann, *et al.*, "Robust Window Discriminator for Photon-Counting Pixel Detectors," *IEE Proceedings of Optoelectronics*, Vol. 149, No. 2. April 2002.

[3] K. Wayne Current, "Current-Mode CMOS Multiple-Valued Logic Circuits," in *IEEE Journal of Solid-State Circuits.* Vol. 29, No. 2. February 1994.

[4] Klaas Bult, and Govert Geelen, "An Inherently Linear and Compact MOST-Only Current-Division Technique", *IEEE JSSC,* Vol. 27, No.12, pp. 1730-1735, Dec. 1992.

Dr. Amit Kr. Jain is Director / Professor / Advisor as well as Founder Director of various Centres /Institutions.

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