An Efficient Carry Select Adder–A Review

Rishabh Rai[1] and **Rajni Parashar**[2]

Department of Electronics & Communication Engineering, Ajay Kumar Garg Engineering College, Ghaziabad 201 009 UP, India.

[1]rishabh.rahul001@gmail.com ,[2]2401.rajni@gmail.com

Abstract -- **Adders are one of the widely used digital components in digital integrated circuit design. Generally,addition is the basic operation which isused in almost all calculation and computational systems. So, the efficient implementation and design of arithmetic units requires the binary adder structures to be implemented efficiently. A ripple carry adder has smaller area in design while it has less speed. A carry look ahead adder is faster in operation as its area requirements are high. Carry select adders lie in between the spectrum. Design of highly efficient Carry Select Adder using Square-root technique suggests many opportunities for increasing the speed and reducing the area of any data processor. Generally, we have the carry select adder (CSLA), the fastest adder which is used in many data-processing processors to perform fast arithmetic operations. If we study the structure of CSLA, we come to know that there is scope in area reduction and delay. In this study, a carry select adder for the computational process is explained which has some modules to be implemented and synthesized using HDL coding. Carry select adder (CSLA) is one of the fastest adder in comparison to all other adders. This review undergoes very simple and efficient gate-level modification to reduce the area and delay of the CSLA. Based on this modification, 8-bit, 16-bit, 32-bit and 64-bit Square-Root CSLA (SQRT CSLA) architecture have been developed having comparison with the regular SQRT CSLA architecture. The proposed circuit design has reduced area and delay as compared with the regular SQRT CSLA.**

Keywords: *CSLA, RCA, BEC*

I. INTRODUCTION

IN recent years, the increasing demand for high-speed arithmetic units in micro-processors, image processing units and DSP chips has paved the path for development of high-speed adders as addition is an important operation in almost every arithmetic unit, and it too acts as the general building block for synthesis of all other arithmetic computations. If we have to increase the portability of systems as well as the reliability of the battery, area and power are the critical aspects which are generally considered. In digital adders and corresponding circuit designs, the speed of addition has somerestrictions by the time required to propagate a carry through the adder. The designs of area and high-speed data path logic systems arethe most important areas of research& study in VLSI system design. In electronic system and applications adders are mostly used. As we know that in microprocessors, one can perform millions of instructions per second. So, the speed of operation is most important factor to be considered while designing multipliers. Even in servers and personal computers (PC), power dissipation is an important design parameter. In today's era, the designs of area-efficient and power-efficient high-speed logic systems are one of the crucial areas of research in VLSI design. In digital adders and circuit design, the speed of addition is limited by the time required by carry to propagate through the adder. The present scenario signifies the field where computations need to be performed using low-power and an area-efficient circuit that must operate at greater speed which is achievable with lesser delay; efficient adder implementation becomes a most important factor as well as the necessity. The example of thedevices like mobile, laptops etc. require more battery usage. So, one who working in the field of VLSI has to optimize these three parameters in a design. These controlling parameters are very difficult to achieve so depending on demand or application some compromise between constraints has to be made.

Ripple Carry Adders have most compact design but they are having slow speed of operation. Whereas, the Carry Look Ahead Adder has fast speed but it consumes more area. Carry Select Adder solves both the problem as generated by that of the Ripple Carry Adder and Carry Look Ahead Adder. A Carry-Select Adder can be structured by using a single Ripple-Carry Adder and an add-one circuit rather than using the dual Ripple-Carry Adders.Based on the area, delay and power consumption requirements, several adder structures have been proposed. A multiplexer-based add-one circuit is proposed to reduce the area with less speed penalty. This acts as the sum for each bit position in an adder which is generated serially only after the previous bit position has been summed and a carry is propagated to the next position.

The CSLA is used in many calculation systems to avoid the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the regular or conventional CSLA is not area efficient as it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by taking carry input C_{in}=0 and C_{in}=1,where the final sum and carry are selected by the multiplexers.

The basic idea of this study is to use Binary to Excess-1 Converter (BEC) rather than that of RCA withC_{in}=1 in the regular CSLA to obtain lower area and delay. As, in BEC logic,lesser number of logic gates are used and hence the circuit is optimized, the modified CSLA is more efficient than that of the regular CSLA.

II. LITERATURE SURVEY

.Much of the research efforts of the past years in the area of digital electronics have been directed towards increasing the speed of digital system.There are different types of fast adders used in processors such as Ripple Carry Adder (RCA),Carry Look Ahead Adder (CLA)and Carry Select Adder. Ripple carry adder generates the compact design but their computation time is high. Carry Look Ahead Adder basically provides fast result but it results in increase in area. Carry Select Adder provides a better approach between RCA and Carry Look Ahead Adder. Ripple Carry Adder generates worst case delay, because it comprises ofN single bit full adders. Each adder gives the sum and carry. The carry generated by the previous full adder is given as the input to the next adder. The carry is transferred through every stage and produces a delay which is called as a worst case delay. In Ripple Carry Adder, as value of N increases, delay also increases.

Recently the requirement of portability and the moderate improvement in battery performance indicates that the power dissipation is one of the most critical design parameter. The three most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation. Portability imposes a strict restriction on power dissipation while still requires high computational speed. Hence, in recent VLSI Systems, the power-delay product becomes the most important aspect of performance. The reduction of the power dissipation and the improvement of speed require optimizations at all levels of the design procedure.

Ripple Carry Adder has the lowest speed among the fast adders. The CSLA is used to find out all possible values of input carry i.e. 0 and 1 and calculates the result in advance. The result is passed through a select line by the multiplexer. The CSLA generallyuses dual RCA's to generate partial sum and carry by considering C_{in}=0 and C_{in}=1 then the final sum and carry is selected by using multiplier. In regular CSLA area consumed is more due to the use of dual RCA's. The basic idea of this study is to use Binary to excess-1 converter (BEC) rather than that of RCA with C_{in}=1 to reduce the area and power. The advantage of BEC is that it requires less number of logic gates than that of the N bit full adders. To reduce the delay, N bit ripple carry adders are replaced with N+1 bit BEC.So, the newly modified Sqrt. CSLA is area consuming than regular CSLA.

Since, most digital circuitry comprises of simple and/or complex gates; we study the best way to implement adders in order to attain low power dissipation and high speed. Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry, i.e. C_{out} of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Figure 1 shows the block diagram of Ripple Carry Adder (RCA). Now, as the value of N increases, delay of adder increases linearly. So, RCA has the slowest speed amongst all adders because of large propagationdelay, but it occupies the least area. Now CSLA provides a way to get around this linear dependency to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage. So,the conventional CSLA makes use of dual RCA's to producethe partial sum and carry by taking the input carry C_{in} = 0 and C_{in} = 1, then the final sum and carry are selected by multiplexers. Figure 2 shows the 16-bit SQRT. CSLA.The Sqrt. CSLA is area consuming due to the use of dual RCA's.

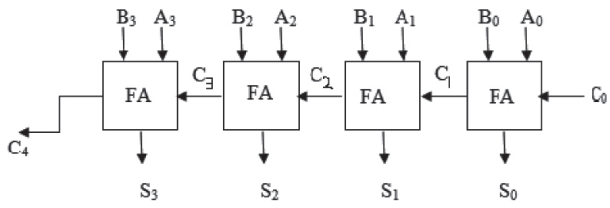

Figure 1. Four-Bit Ripple Carry Adder.

SQRT CSLA has been chosen for comparison with modified design using BEC as it has more balanced delay, less area and low power [4]. Regular SQRT CSLA also uses dual RCAs. In order to reduce the delay, area and power, the design is modified by using BEC instead of RCA with Cin=1. Therefore, the modified SQRT CSLA occupies less area, delay and low power. Further, the parameters like delay, area and power can be reduced.

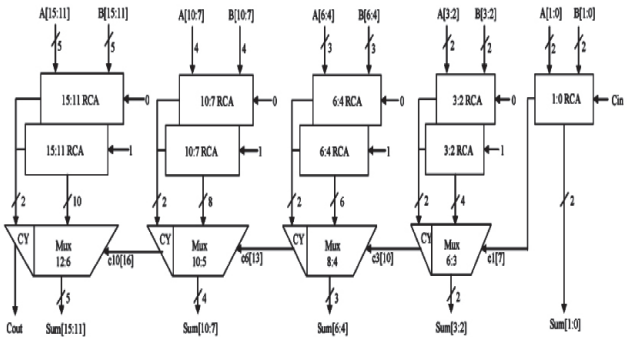

Figure 2. Sixteen-Bit Regular SQRT CSLA.

A conventional carry select adder is a configuration of dual RCA in which one RCA generates sum and carry output by

assuming C_{in} = 0and the other RCA produce carry and sum and sum assuming C_{in} = 1 [3]. This conventional carry select adder has less carry propagation delay than conventional RCA adder but increases the complexity due to dual RCA structure. A carry select adder generating carry of block with carry in as1 from the block with carry in as 0 was proposed by Tyagi.[13] in 1990. Later in 1998, Chang and Hsiao[10] proposed a carry select adder consisting of single ripple carry adder. This was a real start in the carry select adder history.In 2001 a further modified carry select adder with increased delay but reduced area and power was givenby Kim and Kim [11]. Here the RCA section with C_{in} = 1 was replaced using an add one circuit using multiplexer (MUX). Later in the year 2005 a further modified carry select adder which reduces the area and power consumption was proposed by Amelifard, Fallah and Pedram[12]. It reduces the gap between carry select adder and ripple carry adder.

Later a Sqrt. CSLA was proposed which helps in implementing large bit width adders with less delay. In this system the CSLA's with increasing bit widths are cascaded with each other. It helps in minimizingthe overall adder delay. A BEC based CSLA was further proposed byRamkumar and Kittur[1] which had fewer resources than conventional CSLA but with more delay. A CBL (common Boolean logic) based CSLA[10] was also proposed which requires less logic resources but CPD(carry propagation delay) was similar to that of RCA. A CBL based Sqrt. CSLA [11] was also proposed but the design requires more logic resource and delay than BEC based Sqrt. CSLA.

Now a further modification of CSLA called Area-Delay-Power Efficient Carry Select Adder [1] was proposed. Here the carry generation is faster but the area consumption is not much reduced. The carry of the system is calculated before the sum generation.Also the carry generation unit was also replaced using an optimized logic.Thus the system has lesser carry output delay than all other system. Though the carry generation is faster, the area and power consumption are not much reduced. So a further modification with a reduction in area and power consumption, thus obtaining an optimized area-delay and power carry efficient carry select adder is proposed here.

The CSLA[1] is used in many computational systems to remove the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [3]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input C_{in}=0 and C_{in}=1, then the final sum and carry are selected by the multiplexers.The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [6].In particular; Carry-Propagation Adder (CPA) is frequently part of the critical delay path limiting the overall system performance due to the inevitable carry propagation chain. For example, the delay of a fast CPA for converting the final carry-saved number to its two's complement form in a Wallace tree multiplier is typically 25% to 35% of the total multiplier delay [10].Power is an important factor for which power optimization refers to number of Joules dissipated over a certain amount of time whereas energy is the measure of the total number of Joules dissipated by a circuit. In digital CMOS[2] design, the well-known power-delay product is commonly used to assess the merits of designs. In a sense, this can be shown as power × delay = (energy/ delay) × delay = energy, which implies delay is irrelevant.Bedrij (1971) [7] suggested that the propagation delay can be reduced by independently generating multiple carries and using these carries to generate simultaneously by generating sums. Ramkumar and Kannan [1] proposed that a BEC to reduce the maximum delay of carry propagation in final stage of Carry Save Adder. Chang and Hsiao [10] proposed the implementation of low power and area efficient carry select adder using D-Latch instead of BEC. Kim and Kim [11] proposed BEC technique which is a simple and gate level efficient modification to significantly reduce the area and power of SQRT CSLA. The proposed model uses BEC instead of RCA which is used in regular CSLA.

III. RIPPLE CARRY ADDER (RCA)

Ripple carry adder is logical circuit using multiple full adders to add N-bit numbers. Each full adder provides the input as C_{in}, which is the C_{out} of the previous adder. This kind of adder is known as a ripple carry adder, since each carry bit "ripples" to the next full adder. The sum and the output carry of any stage cannot be produced until the carry input occurs which causes a time delay in the addition process. The carry propagation delay for each full adder as shown in Figure 3 is a time from the application of the input carries until the output carry occurs.

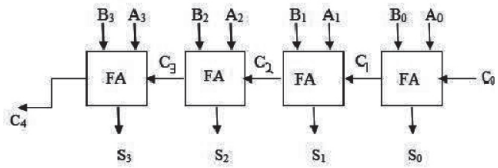

Figure 3. Four-Bit Ripple Carry Adder.

The Ripple Carry Adder [1, 2] is used for evaluating addition of two N-bit numbers. For addition of N-bit numbers, N full adders are needed. From the second full adder carry input of every full adder is the carry output of its previous full adder. This kind of adder is stated as Ripple Carry Adder because of rippling of carry to next full adder is governed here. The general structure of full adder is shown in Figure4.

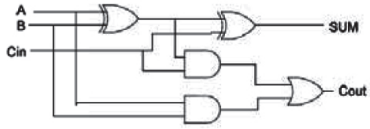

Figure 4. Basic Diagram of Full Adder.

Using the equation C_{in} = Gn-1+Pn-1Cn-1, conventional Ripple Carry Adder is structured. Here each stage uses the output of the previous stage. The delay is directly proportional to the number of bits as shown in Figure 5. This adder undertakes the minimum number of logic gates and the worst case delay is generally more. It is suggested that the adder has a regular layout and uses 5 logic gates per bit. For an n bit adder total number of logic gates used is 5n and the delay is 2n+2 logic gates. For area calculation only two input AND, OR and XOR gates are considered.

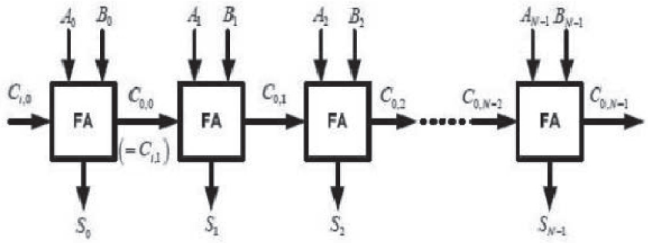

Figure 5. Block Diagram of Four-Bit Ripple Carry Adder.

Half Adders are used to add two one bit binary numbers. It is also possible to structure a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs a$\mathbf{C_{in}}$**,** which is the $\mathbf{C_{out}}$ of the previous adder. This kind of adder is a **ripple carry adder,** since each carry bit "ripples" to the next full adder. The first (and only the first) full adder may be replaced by a half adder.

IV. CARRY SELECT ADDER

Carry Select Adder is a fast adder which is used in digital communication and Memory Architectures as shown in Figure 6. The Carry of one ripple carry adder will be '0' and another will be '1'.Here the output sum and carry is identified by the 2 to 1 multiplexers. The control signal of the multiplexer can be represented by carry (C_{in}).

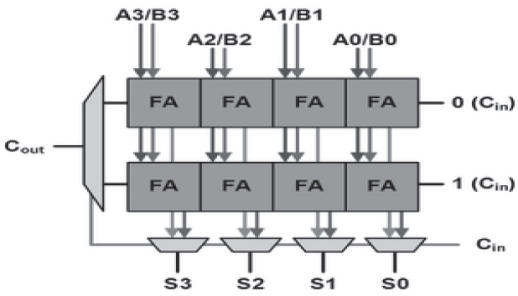

Figure 6. Basic Carry Select Adder Circuit.

The Carry Select Adders are divided into two types: Uniform sized adders and variable sized adders. When thebit length is equally divided it is stated as an uniform sized adder. It is also called as the linear Carry Select Adder. In variable sized adders the bit lengths are generally unequally divided. It is also called SQRT Carry Select Adder (CSLA). Normally the CSLA is designed with the dual Ripple Carry Adders with the carry being '1' and '0'.Here, rather than that of having dual ripple carry we are having only single ripple carry adder while the binary to excess one converter is connected instead of RCA with Carry '1'.[8]-[12].

The block diagram of conventional Carry Select Adder (CSLA) [1] is shown in Figure 7. CSLA uses RCA to generate sum and carry values using initial carry as 0 and 1 respectively, before the actually carry arrives in. Upper RCA is given with carry initial value as logic "0" while lower RCA is given with carry initial value as logic "1". Multiplexer selects the result of carry "0" path if the previous carry is logic '0' or the result of carry "1" path if the previous carry is logic '1 i.e. actual carry is used to select the sum and carry using a multiplexer.

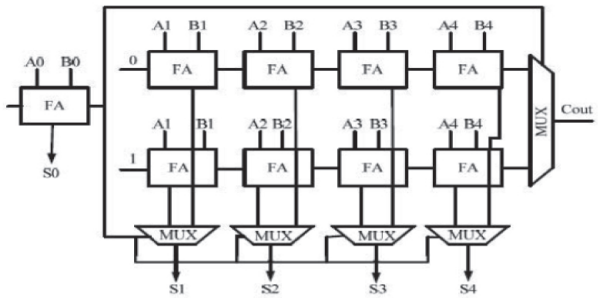

Figure 7. Block Diagram of Conventional CSLA.

Each RCA pair in CSLA can compute in parallel the value of sum before the previous stage carry comes. Thus, the critical path of an N bit adder is reduced. Delay in CSLA is much lesser than RCA because the critical path in case of conventional adder is N-bit carry propagation path and one sum generating stage while in case of CSLA, the critical path is (N/L)-bit carry propagation path and L stage multiplexer with one sum generating stage in the N- bit CSLA, where L is number of stages in CSLA as shown in Figure 7. Since L is much less thanN and multiplexer delay is less than the delay in full adder, hence the delay in the CSLA is much less than that in the RCA but there exists copy of hardware in each stage which leads to an increase in the amount of power consumption and cost.

V. BASIC ADDER BLOCK

The adder block using a Ripple carry adder, BEC and Mux is described in this section. In this, we explain the delay & area using the theoretical approach and show how the delay and area effect the total implementation. The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Figure 8. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay of 1 unit and area of 1 unit. We can then add up the number of gates in the longest path of a logic block that contributes to

the maximum delay. The area evaluation is calculated by counting the total number of AOI gates required for each logic block. Based on this method, the blocks of 2:1 mux, Half Adder (HA), and Full Adder (FA) are evaluated and listed in Table 1.

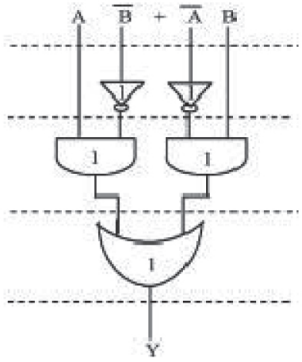

Figure 8. Delay and Area Evaluation of XOR.

Table 1—DELAY AND AREA EVALUATION OF CSLA

Design	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

The next figure i.e. Figure 9 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the Mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control or carry signal C_{in}.

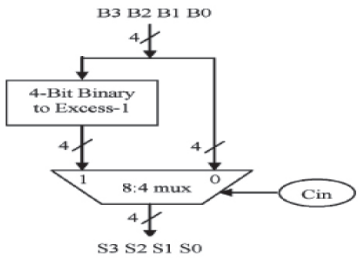

Figure 9. Four-Bit BEC with 8:4 MUX.

VI. BINARY TO EXCESS-1 CONVERTER (BEC)

The general aspect is to use Binary to Excess-1 Converter (BEC) in the regular CSLA to attain lower area and increased speed of operation. This logic is replaced in RCA with C_{in} = 1. This logic can be applied for different bits which are used in the modified design. The main benefit of this BEC logic arrives from the fact that it uses lesser number of logic gates than the n-bit Full Adder (FA) structure. As stated above the main idea of this task is to use BEC instead of the RCA with C_{in}=1 in order to reduce the area and increase the speed of operation in the regular CSLA to obtain modified CSLA. To replace the n-bit RCA, n+1 bit BEC logic is required as shown in Figure 10. Figure 11 shows the BEC using carry out.

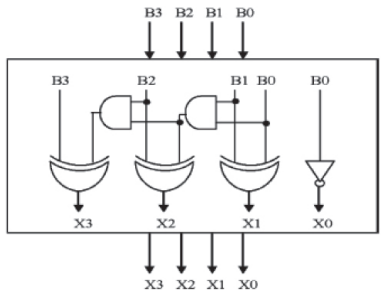

Figure 10. Four-Bit Binary to Excess-1 Converter.

The Boolean expressions of the 4-bit BEC is given as (note the functional symbols! NOT, & AND, ^XOR).

X0 =! B0
X1 = B0^B1
X2 = B2^ (B0 & B1)
X3 = B3^ (B0 & B1 & B2)

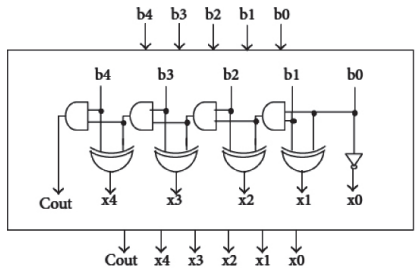

Figure 11. Four-Bit Binary to Excess-1 Converter Using Carry Out.

The respective block level implementation includes the Ripple Carry adder, BEC unit as well as the sum and the carry selection unit, which are accordingly connected to each other with the marked bits such as 0 as well as the carry in and carry out. The respective order of n signifies the level of bits such as 1, 2etc. as shown in the Figure 12. Here, at the output section, the sums as well as the carry units are accordingly generated.The truth table of 4-bit binary to excess - 1 logic is respectively shown in the Table 2.

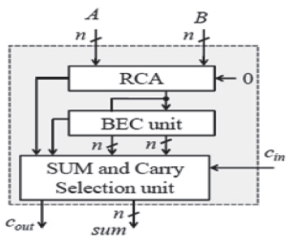

Figure 12. Connection of RCA, BEC and Sum & Carry Block

TABLE 2—TRUTH TABLE OF FOUR-BIT BEC

Binary Logic B0 B1 B2 B3	Excess-1 Logic E0 E1 E2 E3
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

VII. MODERN APPROACH

This architecture is similar to regular 16-bit SQRT CSLA, the only change is that, we replace RCA with C_{in}=1 among the two available RCAs in a group with a BEC. This BEC has a feature that it can perform the similar operation as that of the replaced RCA with C_{in}=1. Figure 13 shows the modified block diagram of 16-bit SQRT CSLA. The number of bits required for BEC logic is 1 bit more than that of the RCA bits. The modified block diagram [1] is also divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding mux. Thus, the sum1 and carry 1 (output from mux) are depending on mux and resultscomputed by RCA and BEC respectively. The sum2 depends on carry 1 and mux. For the remaining parts the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's.

III. DISCUSSION OF RESULTS

The results from the galvanostatic charge/ discharge showed how the current and voltage in a capacitor are. When one of them rose, the other one also rises and vice versa as shown in figure 2. The charge energy also depended on them as shown in figure 3. The capacitance of the supercapacitor was observed to also change during the charging and discharging periods. It increased while charging and decreased while discharging. This is not in conformity with equation 3 in which the capacitance is considered to be constant.

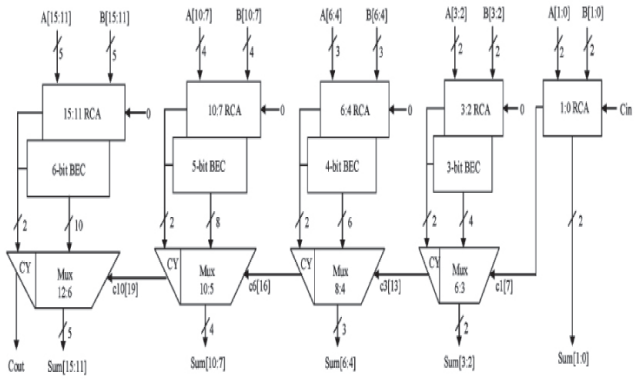

Figure 13. Sixteen-Bit Regular SQRT CSLA.

Basically, the proposed structure of the modified CSLA will contain the design specification of the NAND Gate instead of the NOR Gate. As a result, the number of gates will be reduced and hence the parameters such as area. The delay of the proposed circuit will also be getting affected.The comparison of the RCA &CSLA in terms of the delay as well size parameters denoted in the form of n is shown in table 3.

Table 3--COMPARISON TABLE OF RCA & CSLA

ADDER	DELAY	SIZE
RCA	N	N
CSLA		2N

VIII. CONCLUSION

Power, delay and area are the main performance parameters of CSLA and the reduction of these parameters is the challenging issue of today's VLSI research. Many methods and techniques have been proposed to design fast, compact and less power consuming CSLA. But as we can analyze from the recent method proposed that there is a trade-off between area consumption and delay of CSLA. Therefore, there is a scope to make CSLA more delay and area efficient by optimizing the circuit. The overall improvement in Modified CSLA shows better results in terms of area power and delay. Hence, proposed modified CSLA is being used for power and area efficient devices.

IX. ACKNOWLEDGEMENT

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Rishabh Rai is pursuing M.Tech (2013-15) from Ajay Kumar Garg Engineering College,Ghaziabad (affiliated to Uttar Pradesh Technical University,Lucknow) in VLSI Design. His areas of interest are Digital System Design,Embedded System Design, & Low Power VLSI Design.He completed his B.Techfrom Vishveshwarya Institute of Engineering & Technology, Gr.Noida (affiliated to Uttar Pradesh Technical University, Lucknow) in Electronics and Telecommunication Engineering with Honours in the year 2013. During his career he has been appreciated and certified for securing Rank in Top Five Positions in the respective branch for consecutive four years during B.Tech and Amul Vidya Bhushan Award for his performance in AISSCE-2009,at the District Level. During his graduation, he has also been awarded with the Best Paper Presentation in the IEEE Sponsored National Conference, ETEAT-2013. He is the student member of IEEE.

Rajni Parashar is currently working as an Assistant Professor in Department of Electronics and Communication Engineering with Ajay Kumar Garg Engineering College,Ghaziabad (affiliated to Uttar Pradesh Technical University, Lucknow). She completed her B.Tech from Punjab Technical University, Jalandhar and M.Tech from Kurukshetra University, Kurukshetra. She has four years of teaching experience and six months of industrial experience to her credit. Her research interests are in the areas of Digital and Analog Circuit Design & Microelectronics.