FPGA Realization of Double Data Rate Synchronous Dynamic Random Access Memory Controller

Dipa Nitin Kokane
Department of Electronics and Communication Engineering, ABES Engineering College, Ghaziabad 201009 UP India
dipbanait@rediffmail.com

Abstract -- **The DDR SDRAM controller provides the user with a simplified interface to a industry standard memory device. Using this controller makes access to DDR SDRAM devices as simple as possible. This application note describes a DDR SDRAM controller design implemented in vertex-II device. It targets a DDR SDRAM device at a clock rate of 200 MHz with data transfer at 400 MB/s. In this design, the memory controller is used to perform the correct initialization sequence and to transmit to the SDRAM device, through the appropriate sequence of control and data signals. The read and write command receives from user interface and transmits to DDR SDRAM through controller.**

Keywords: .SDRAM, DDR, DLL, DQS, DCM

I. INTRODUCTION

WITH microprocessors getting faster every year, memory architecture must also improve to enhance the overall system performance. DDR SDRAM is the top contender for this next generation of SDRAM. DDR SDRAM was approved as a JEDEC Standard in Feb 1998.

It is obvious that bus speeds will need to increase well beyond that in order for memory bandwidth to keep up with future processors. There are several competing new standards on the horizons that are very promising; however most of them require special pinots, smaller bus widths, or other design considerations. In the short term, Double Data Rate SDRAM looks very appealing. Essentially, this design allows the activation of output operations on the chip to occur on both the rising and falling edge of the clock. Currently, only the rising edge signals an event to occur, so the DDR SDRAM design can effectively double the speed of operation up to at least 200MHz.

II. DDR SDRAM OVERVIEW

The 128Mb (x32) DDR SDRAM is a high-speed CMOS, dynamic random access memory containing134,217,728- bits. It is internally configured as a quad bank DRAM. All the inputs are compatible with the JEDEC SSTL_2 standard and all outputs are SSTL_II class II compatible.

The 128Mb DDR SDRAM uses double data rate architecture to achieve high-speed operation. A bi-directional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command is used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

DDR SDRAM provides locations for 2, 4, 8, or full page programmable read or write burst. An auto precharge function can be enabled to provide a self-timed precharge that is initiated at the end of burst access.

Memory controller features:

1) Support 2, 4, 8 burst length.
2) Uses CAS latency 3.
3) Target 200 MHz DDR SDRAM
4) Data transfer rate at 400 MHz.

Memory Initialization: The memory must be powered up and initialized in a predefined manner. The initialization.

Sequence is handled by the controller, as follows:

1. After all power supply and reference voltages are stable and the clock is stable, the DDR SDRAM requires a 200 µs delay prior to applying an executable command.
2. Once the 200 µs delay has passed, the initialization sequence begins:
   a. A DESELECT or NOP command is applied and CKE is set High.
   b. A PRECHARGE ALL command is applied.

c. A LOAD MODE REGISTER command is issued for the extended mode register to enable the DLL.
d. Another LOAD MODE REGISTER command is issued to the mode register to reset the DLL and to program the operating parameters.
e. A PRECHARGE ALL command is applied, placing the device in an all-banks-idle state.
f. Once in the IDLE state, two AUTO REFRESH cycles are performed. Two hundred clock cycles are required between the DLL reset and any Read command.

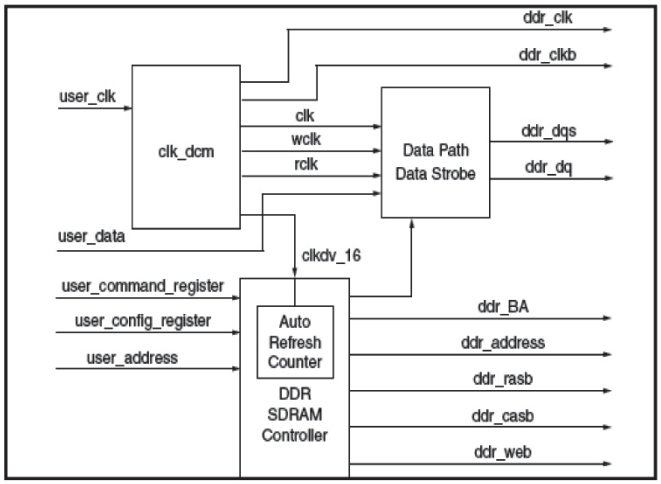


Figure 1. Block diagram of Controller.

AUTO REFRESH Counter: The memory requires AUTO REFRESH cycles at an average interval of 15.6 µs clock divided from the system clock of 200 MHz is used in a counter to generate the AUTO REFRESH cycles.

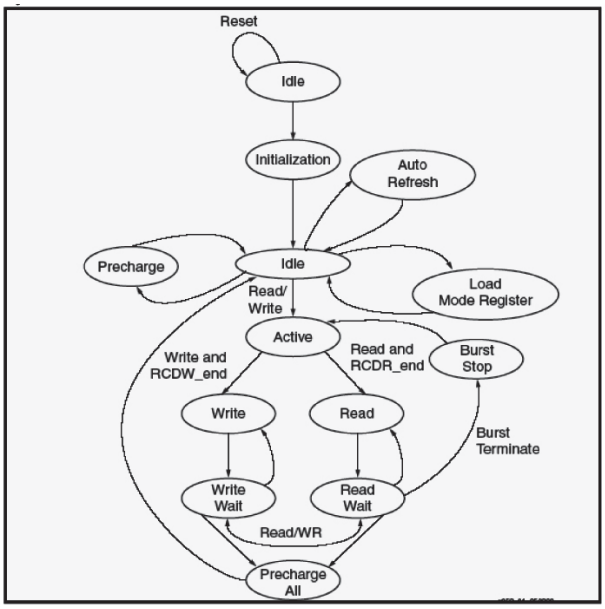


Figure 2. DDR SDRAM Controller State Machine.

Clocking Methodology: This section describes the clocking methodology implemented in this design. The first DCM generates CLK0 and CLK90. CLK0 directly follows the user-supplied input clock. This DCM also supplies the CLKDV output, which is the input clock divided by 16 used for the AUTO REFRESH counter. Figure 3 is the DCM implementation.

The second DCM in the controller (DCM2_RECAPTURE) generates a phase-shifted version of the user input clock. It is used to recapture data from the DQS clock domain during a memory Read.When adequate DCM resources are available. A third DCM can be used for better timing margins. This DCM is used to generate WCLK, a phase shifted version of the system clock. WCLK is used to clock data at the DDR IOB registers during a Write.

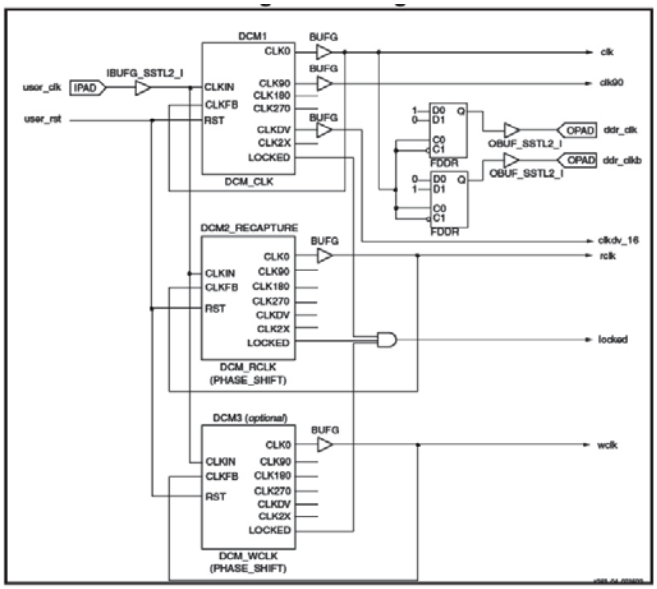


Figure 3. DCM.

Read Data Path: Figure 4 shows the block diagram of data path. During Read cycles, the memory provides DQS edge aligned with the Data to the controller. This design uses DQS to capture data provided by the memory. Because DQS is strobing in nature, data captured on the DQS domain needs to be recaptured. The Dqs_enable signal controls the 3-state output while the dqs_reset holds DQS flip flop in reset. The dqs_reset helps to meet the Write preamble timing required by the memory.

Write Data Path: During a memory Write, the controller must make sure the Data Strobe (DQS) is center aligned with the data at the pins of the DDR SDRAM device. In order to minimize skew, both CLK and DQS are forwarded through the DDR IOB flip-flops. The controller block generates the dqs_enable and the dqs_reset signal required at the IOB flip-flop.

Data Recapture: In order to recapture data, a relationship between the DQS domain and the system clock domain must be found. The reference design uses a phase shifted version of the system clock (rclk) to recapture data from the DQS domain. Data in the DQS domain is written into an asynchronous FIFO built using LUT RAMs. The phase shifted clock, rclk is used to write the data into the FIFO. The data is then read using the system clock (CLK) to convert the data into the system clock domain.

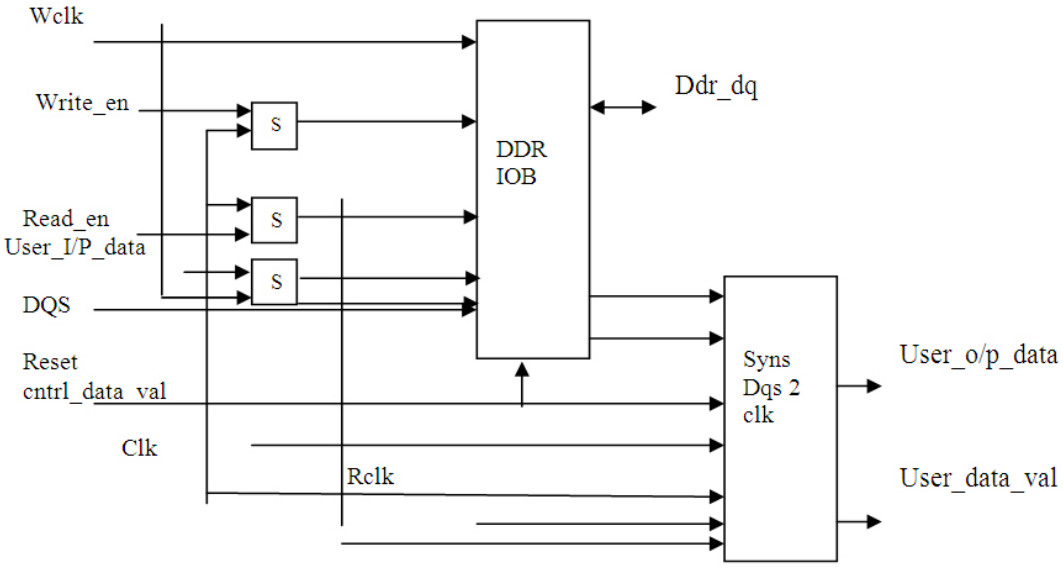


Figure 4. Data Path.

III. SIMULATION RESULTS

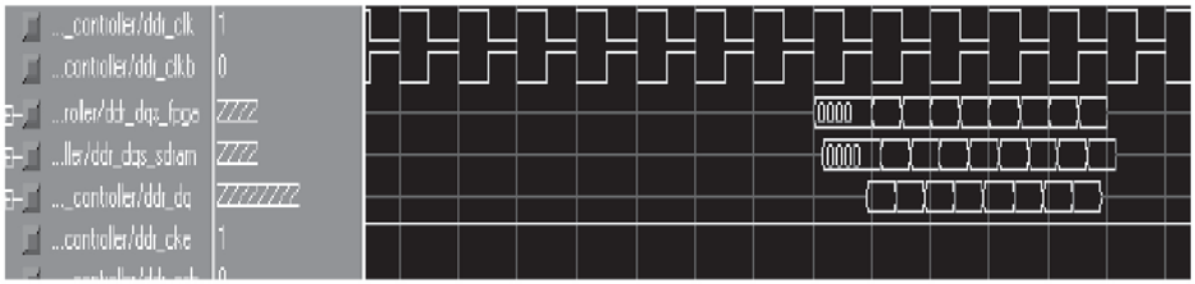


Figure.5 Write of burst length 2.

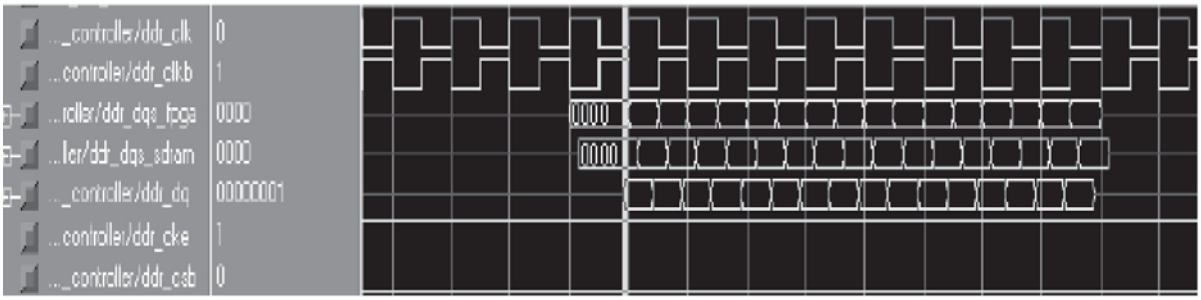


Figure 6. Write of burst length 4.

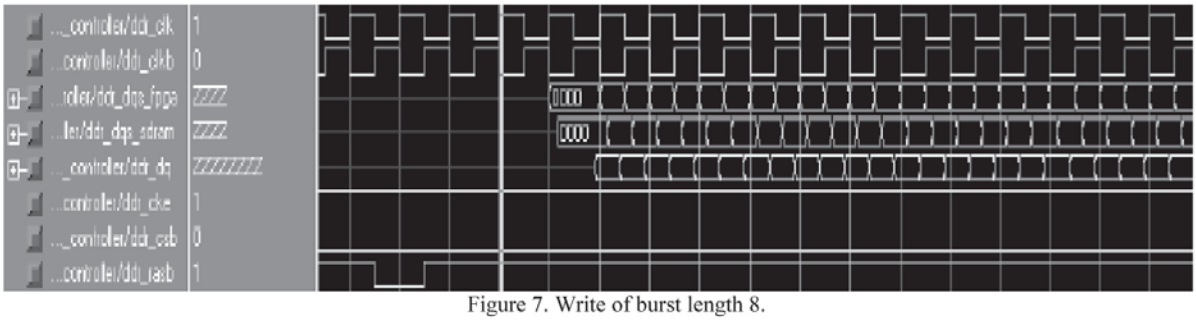


Figure 7. Write of burst length 8.

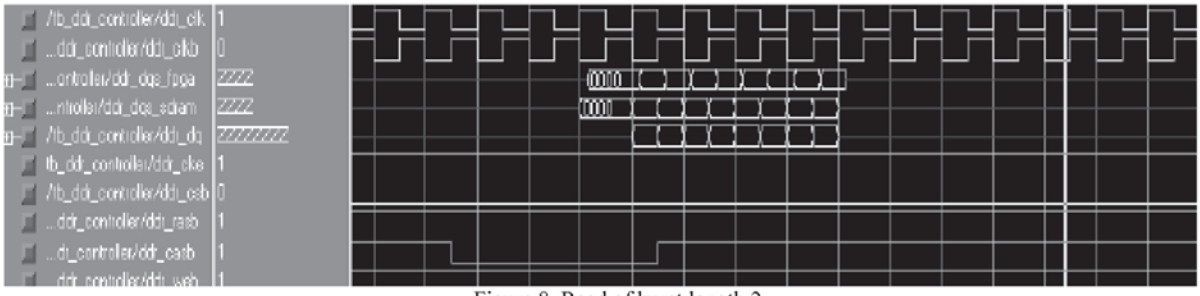


Figure 8. Read of burst length 2.

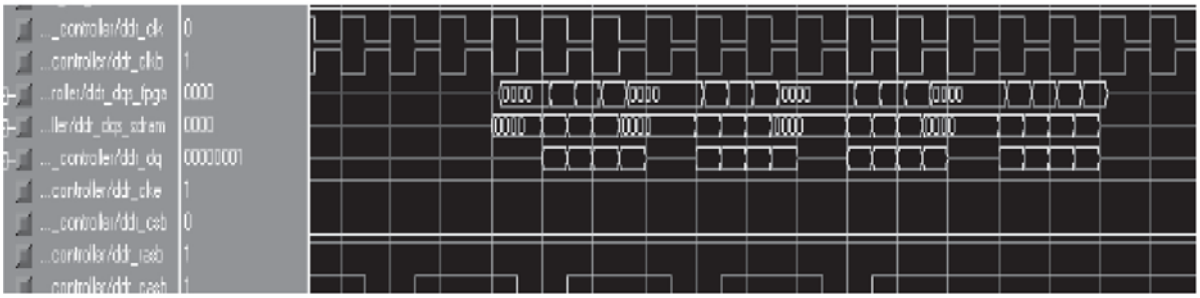
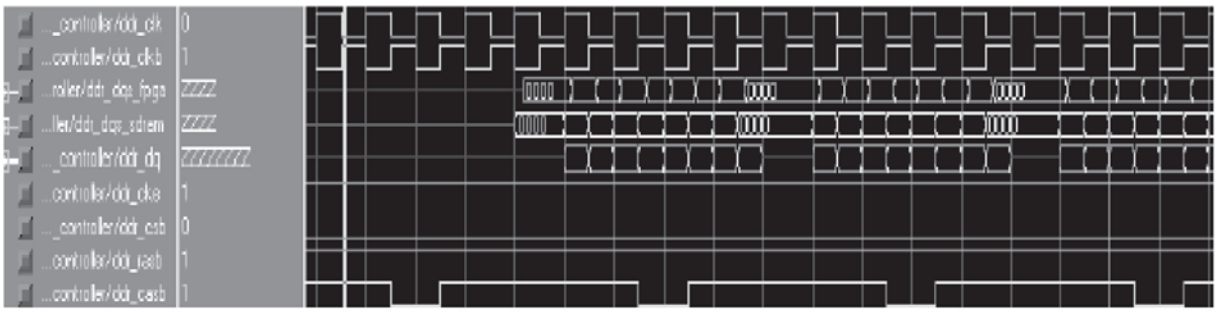


Figure 9: Read of burst length 4.



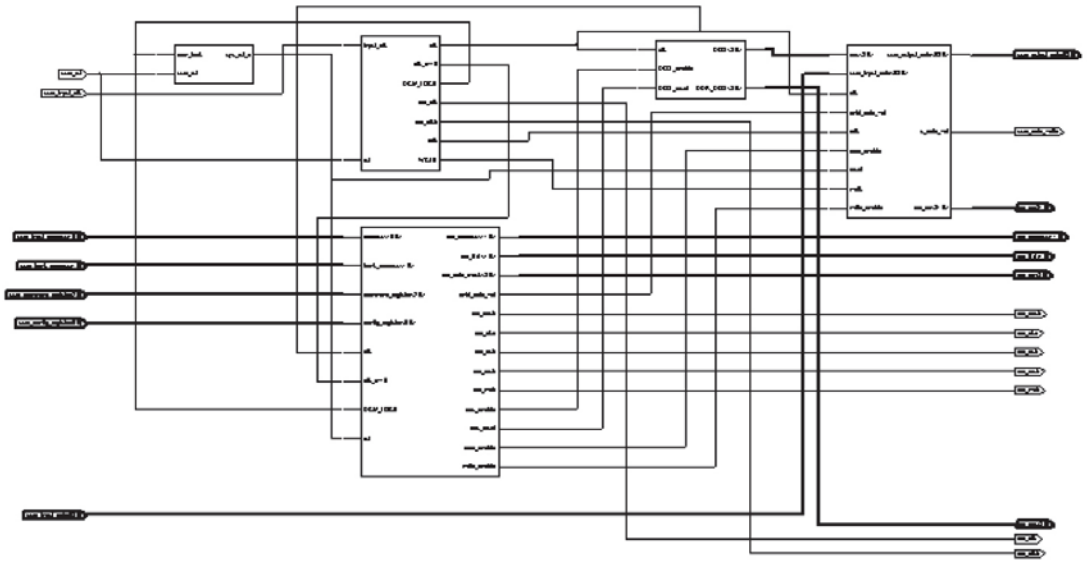


Figure 11. Synthesis Result of Developed Controller.

IV. RESULTS

Here the simulation has performed on each block and the performance has successfully investigated. After mapping all banks together again simulation has performed on complete controller Performance of controller has checked out by applying several commands. After simulation synthesis has performed. Figure 11 shows the simulated and synthesized results of controller.

V. REFERENCES

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Dipa Nitin Kokane is working as Senior Assistant professor in ABES Engineering College, Ghaziabad, India. Obtained M.E. degree from S.S.G.M.M.C.E. College, Amravati University, Maharashtra, India in 2004 specialising in Digital Electronics and B.E. from the same College in 2002 in Electronics and Communication. She has intense passion for teaching. Her field of interest is wireless communication.